1. (Amended) A method of adjusting data timing in a memory system having a memory device and a memory controller, the system operating according to a master clock signal, the method comprising the steps of:

establishing an initial output timing at the memory device;

[transmitting a first set of data from the memory device to the memory controller according to the initial output timing;]

transmitting an echo clock signal from the memory device to the memory controller according to the initial output timing;

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receiving the echo clock signal at the memory controller;

identifying a phase error of the received echo clock signal relative to the master clock signal;

transmitting control data from the memory controller to the memory device for revising the initial output timing in response to the identified phase error to produce a revised output timing; [and]

revising the initial output timing at the memory device according to the control data; and

transmitting a second set of data from the memory device to the memory controller according to the revised output timing.

6. (Amended) A method of controlling data flow in a memory system including a memory controller and a memory device, the method comprising the steps of:

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generating a master clock signal;

transmitting the master clock signal from the memory controller to the memory device;

issuing a first read command to the memory device;

[reading a first set of data from the memory device in response to the read command;]

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producing an echo signal at the memory device in response to the first read command, the echo signal having a phase shift relative to the master clock signal;

transmitting the first set of data to the memory controller with a time delay relative to the echo signal;

transmitting the echo signal to the memory controller;

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receiving the echo signal at the memory controller;

comparing the received echo signal to the master clock signal;

selecting an adjusted time delay in response to the step of comparing the received echo signal to the master clock signal;

issuing a second read command to the memory device;

reading a second set of data in response to the second read command; and

transmitting to the memory controller the second set of data with the adjusted time delay.

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11. (Amended) The memory controller of claim 10 wherein the phase comparator includes:

a signal source having a plurality of outputs and operative to produce a plurality of phase-shifted signals at the outputs in response to the master clock signal; and

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a plurality of phase comparator, each phase comparator including a first input coupled to the signal source outputs, a second input coupled to the clock bus <u>to receive echo signals</u> and a phase output coupled to the logic circuit.

12. (Amended) The memory controller of claim <u>11</u> [6] wherein the signal source includes a multiple output delay-locked loop.

13. (Amended) A memory system, comprising:

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a command bus;

a clock bus;

a data bus;

a memory controller including a master clock generator coupled to the clock bus to generate a master clock signal, a phase comparator having a first input coupled to the master clock generator and a second input and responsive to a phase difference between the first and second inputs to produce an adjust command, and a logic circuit; and

a memory device having a clock input coupled to the clock bus, an echo signal generator to generate an echo signal responsive to the master clock signal at the clock input, the echo signal generator being coupled to the second input of the phase comparator, a data latch having a trigger input and responsive to a control signal at the trigger's input to transmit data to the data bus, and a variable delay circuit having a control output coupled to the trigger input and a command input coupled to the command bus, the delay circuit being responsive to the adjust command on the command bus to produce the control signal at a time [a delay] corresponding to the adjust command.

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14. (Amended) The memory system of claim 13 wherein the phase comparator includes:

a signal source having a plurality of outputs and operative to produce a plurality of phase-shifted signals at the outputs in response to the master clock signal; and

a plurality of phase comparator, each phase comparator including a first input coupled to the signal source outputs, a second input coupled to the echo signal generator [clock bus] and a phase output coupled to the logic circuit.

Please add new claims 16-19 as follows:

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-- 16. A method of adjusting data timing in a memory system having a memory device and a memory controller, the method comprising the steps of:

transmitting a first set of data to the memory device according to a first clock signal;

receiving the first set of data at the memory device;

establishing an initial output timing at the memory device having a default phase relationship with the first clock signal;

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transmitting a second set of data from the memory device to the memory controller according to the initial output timing;

receiving the second set of data at the memory controller;

comparing the second set of data to the first clock signal in order to identify a phase error;

transmitting a third set of data from the memory controller to the memory device for revising the initial output timing in response to the identified phase error; and

revising the initial output timing at the memory device according to the third set of data to produce a revised output timing.

17. The method of adjusting data timing according to claim 16 wherein the step of transmitting a second set of data includes transmitting an echo clock signal.

18. The method of adjusting data timing according to claim 17 wherein the step of comparing the second set of data comprises the steps of:

generating a plurality of phase shifted signals responsive to the first clock signal;

comparing the echo clock signal to each of the phase shifted signals;

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